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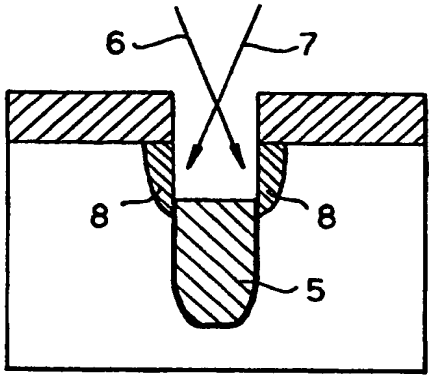
(57) Abstract

A method of forming a doped trench as part of the fabrication of a semiconductor device such as a trench gated power device, logic transistor or memory cell. A trench (3) is formed in a semiconductor substrate (1) using a mask (2). The trench is partially filled with electrode material (5) and the side walls of the trench are doped with the mask (2) still in place.



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SEMICONDUCTOR DEVICE FABRICATION

The present invention relates to a method of forming a doped trench as part of the fabrication of a semiconductor device.

A first conventional method of forming a doped trench is to implant a semiconductor with a suitable dopant and then etching through the implanted region to leave a trench with two side lobes. This method results in a doping profile as shown in the graph of Figure 13. It can be seen from Figure 13 that this doping method is characterised by a gradual drop off in concentration in both directions. This method has the disadvantage that the bottom of the doped region generally will not align with the electrode material which is added to the trench at a later stage.

US-A-4415371 describes a second conventional method of fabricating a sub-micron dimension NPN lateral transistor. An array of hundreds of devices may be simultaneously processed on a chip to sub-micron dimensions by establishing tiny active regions for each transistor surrounded by field oxide field trenches which are utilized to dope the substrate within the action region. n+ regions are implanted in the trench by ion implanting at a large angle. The angle of the ion beams relative to the trench direction ensures that the n+ implanting does not extend to the full depth of the trench. This is due to a shadowing effect.

A disadvantage of this device is that the large ion implanting angle (which is necessary to ensure that the trenches are not fully doped) is non-standard and expensive, and also ionic reflections will reduce the effectiveness of the shadowing. Also the doped region will generally not align with the top of the electrode material which is deposited at a later stage.

In accordance with the present invention we provide a method of forming a doped trench as part of the fabrication of a semiconductor device, the method comprising:

(i) forming a trench in a semiconductor substrate using a mask to define the trench region;

(ii) either

a) filling the trench and removing part of the contents of the trench to leave a partially filled trench; or

b) partially filling the trench; and

(iii) doping the side walls of the trench with the mask still in place.

The trench may be filled in step (ii) with any suitable material, depending on the particular type of semiconductor device being fabricated. Typically the trench is filled with a suitable electrode material or combination of materials as in a silicided gate.

The trench may be fully or partially filled with electrode material in step (ii) a), and then removed down to a desired level in the trench eg. by etching. Alternatively the trench may be partially filled in one step (ii) b) up to the desired level. In this case the trench is typically partially filled by evaporation of eg. aluminium.

The lateral spread of the doping profile can be accurately controlled and can be made to be very narrow. This is highly advantageous where trenches must be placed adjacent and as close as possible to one another and allows a particularly high device density. Conventional transistor arrays exhibit a device density of the order of 4 million devices per square inch. The present invention can be utilised to form a transistor array with approximately 400 million devices per square inch.

Device parameters such as the particular electrode material used and the dopant ions/atoms will depend on the particular device being fabricated. Typically the electrode is polysilicon or any refractory metal. Typically the dopant atoms are arsenic, phosphorous, boron or antimony for silicon, but other elements will be used for other substrate materials.

Preferably the trench is partially filled before the doping step. This ensures that the bottom of the doping profile is self-aligned to the top of the trench filling material (trench refill). Where the trench refill acts as an electrode in the final device, this will help to minimise the capacitance between this electrode and the doping region, and ensures channel continuity in a MOS gated device.

Where the gate is principally polysilicon, the doping step (iii) will also dope the polysilicon. This will enhance the electrode conductivity and therefore its switching speed.

Typically (as in a MOSFET but not in a device such as a MESFET) a dielectric (such as silicon dioxide) will be formed on the surface of the trench between steps (i) and (ii). After step (ii) the dielectric at the upper part of the trench will be exposed. The doping step may then be carried out by penetrating through this layer or alternatively, the exposed dielectric material may be removed beforehand.

Typically, the doping step (iii) comprises introducing dopant ions from an angled ionic source. This can result in very high surface dopant concentrations. This allows very low sheet resistivity regions to be formed. Further, the use of ion implantation means that a rapid thermal anneal can be used which will mean that if the semiconductor device is a power device which is used in a smart power device (where there are other impurity profiles in logic circuits) then this process will be more suitable as it will not affect the previous processing.

The angled implanting step may be carried out with a low angle of implant. This generally means that more than one implanting step could be required to dope all sides of the trench. Alternatively the angle of the ionic source to the surface of the substrate may be increased. The resulting ionic r flections from the side walls of the trench then causes substantially all sides of the trench to

be at least partially doped and generally only one implanting step could be required.

Alternatively, the doping step (iii) may comprise diffusing dopant ions into the sidewalls of the trench from a dopant gas such as arsenic, phosphorous, boron, antimony or any other suitable dopant gas.

Further alternatives for the doping step (iii) include deposition of a dopant source such as heavily doped glass; and filling the exposed part of the trench with spin on dopant. Where the dopant mechanism is from a dielectric source (such as spin on glass or doped silicon dioxide), the material can be conveniently etched back to planarise the trench.

The resulting doped trench can then be utilised in the production of a wide variety of semiconductor devices. Examples of such devices are a trench gated power device such as a power MOSFET, MESFET or a power IGBT, a logic transistor or a memory cell.

The mask which is used to define the trench etch is also used to define the doping area in step (iii). This allows the doping step to be carried out by a variety of techniques such as ion implantation or gaseous diffusion, and any choice of doping (impurity) atoms. A further advantage of using the mask in both steps is that in the field areas (i.e. areas that do not have n+ source regions and where the gate contact will be made) this mask is desirable as it reduces the gate capacitance.

The present invention also extends to a device which has been constructed according to the previously described method. The device typically includes doped regions of the side walls of the trench which have a doping concentration which is substantially uniform in the exposed part of the trench (i.e. the part which is not masked by electrode material after step (ii)). The doped region also typically has a well defined drop-off in concentration at the top of the electrode material.

A number of embodiments of the invention will now be described with reference to the accompanying figures, in which:-

Figure 1 is a cross-section of a masked substrate prepared for trench etch;

Figure 2 is a cross-section of the masked substrate of Figure 1 after trench etching;

Figure 3 is a cross-section of the device of Figure 2 after trench refill, etch back and oxidation;

Figure 3A is a cross-section illustrating an alternative method of partially filling the trench;

Figure 4 is a cross-section of a first doping technique comprising angled implant directly through a thin surface layer;

Figure 5 is a cross-section of a second doping technique comprising angled implant directly into the trench wall;

Figure 6 is a cross-section of a third doping technique with large angle implant;

Figure 7 is a cross-section of a fourth doping technique using a diffusion process;

Figure 8 is a cross-section of a fifth doping technique using a solid dopant source;

Figure 9 is a cross-section of a sixth doping technique using spin-on dopant;

Figure 10 is a cross-section of a power MOSFET device constructed according to the invention;

Figure 11 is a cross-section of a power IGBT device constructed according to the invention;

Figure 12 is a cross-section of a logic transistor or memory cell constructed according to the invention;

Figure 13 is a graph illustrating the doping profile for a conventional non-lateral doped region; and,

Figure 14 is a graph illustrating the doping profile of a laterally doped region according to the present invention.

Three stages in the doping preparation process are shown in Figures 1-3. Starting with a substrate 1 (typically silicon), a mask 2 is used to define areas where trenches will be formed (Figure 1). Depending on the trench etch chemistry, the mask 2 could be composed of one of a number of materials such as photoresist, silicon dioxide or silicon nitride.

The trench 3 (Figure 2) is then etched into the substrate 1 to a depth relevant to the device design. The trench can be etched using a plasma, ion beam , wet, or similar etch technique.

Once the trench has been etched, the next processing steps are dictated by the particular device itself. The doping technique described is applicable to a number of devices, mainly transistors, and it is therefore likely that the next step would be a gate oxidation of the surface of the trench to leave a layer of oxide 4 (Figure 3), followed by the deposition of some kind of gate material 5, e.g. polysilicon, or any refractory metal.

This deposition may then be followed by an etch stage to leave the trench in the half filled state shown in Figure 3. Alternatively the trench may be partially filled in one step as illustrated in Figure 3A, and described below:

(i) The trench 3 is formed as described above but uses a 2 layer mask of silicon nitride 30 and silicon dioxide 31 (siO_2).

(ii) Aluminium 32 is then evaporated into the sample and falls much like snow - giving a "line of sight" covering i.e. not conformal.

(iii) When the sample is placed in a wet solution capable of removing the SiO_2, the SiO_2 layer 31 is removed, along with all of the aluminium on the top of it. This is generally known as a "lift off" process. The nitride layer (still necessary as a

doping mask) is left along with the aluminium at the bottom of the trench.

Typically the gate oxide is created by placing the substrate in a furnace with an atmosphere of oxygen, sometimes mixed with steam, nitrogen or hydrogen chloride. The furnace is typically operated at a temperature of 1000 degrees centigrade and cleanliness is a priority as any contaminants can ruin the electrical properties of the oxide.

This is termed "thermal oxidation" and is the standard technique for creating oxides with good electrical properties (ie. gate dielectrics and not passivation layers such as at the top of the trench). Oxides for other purposes ie. coating and insulating are generally deposited and therefore have poorer electrical properties. the dry method of thermally oxidising yields a better oxide (necessary for the accurate control of turn on voltages and reliability) but is a slower process than wet oxidising (ie. using an atmosphere of oxygen and steam).

Depending on the method of doping taken, this may complete the preparation for the doping step. If the first doping method is used (Figure 4) no further action need take place. However, all of the other processes will be much more effective if the substrate is exposed, probably with an etch process to remove the exposed portion of the oxide layer 4 (ie. above the top of the electrode 5).

The particular doping method chosen will depend on the device type and its specifications.

Six possible doping methods will now be described with reference to Figures 4 to 9.

Referring to the first doping method shown in Figure 4, the lateral doped regions 8 can be implanted directly through the oxide (or other thin layers) into the trench walls by dopant ions 6,7 from an angled, isotropic or divergent source. This has the advantage of having a very narrow lateral spread and removes the need to etch the trench sidewall. However, it is likely that at least two

implants will be needed, one for each side of the trench (at the two angles illustrated by ion beams 6 and 7).

In the second doping method shown in Figure 5, an angled implant 6,7 is again used to inject dopant directly into the trench wall. However, in this case the oxide layer 4 has been removed with an etch (ie. the oxide in the exposed region above the electrode 5 has been removed). As a result lateral profile spreading is much easier to control and predict.

If a large angle implant is used (as illustrated by the ion beams 9 in Figure 6), it is possible to take advantage of ionic reflections 10 to dope both sides of the trench in one step. This has the advantage of reducing the number of implant steps, but has the following disadvantages;

1) doping profiles will probably not be symmetric and,
2) large angle implants are not industry standard and will incur added expense.

Profile matching can be optimized by adjusting the mask layer thickness and the implant angle. The dopant ions could be arsenic, phosphorous, boron or antimony. The substrate crystal orientation will also have an effect on the ionic reflections.

After the doping steps shown in Figures 4-6, a rapid anneal is carried out.

Dopant atoms can be diffused into the trench sidewalls from a carrier gas 11 such as Arsine, Diborane or Phosphine (Figure 7). This has the advantage of being a cheap process but may exhibit lower surface concentrations than implanted profiles, with a consequently lower conductance of the doped regions. The diffusion process is carried out at approximately 1000 degrees centigrade and therefore no separate annealing step is necessary.

The deposition of a dopant source 12 (such as a heavily doped glass e.g. BPSG or PSG or oxide doped with phosphorous or arsenic) allows the easy diffusion of the

dopant into the trench sidewalls (Figure 8). This has the advantage of being cheap and also the dopant source may be etched back to planarise the trench. Doping is followed by a rapid thermal anneal.

Alternatively, a spin on dopant 13 (such as glass doped with arsenic) can be used (Figure 9). This has the advantage of not only providing a good source of dopant, but also is an excellent method of planarizing the trench which will be necessary in many applications. The doping step is followed by an anneal. This method automatically fills the trench with oxide.

Figures 1-9 have illustrated a number of initial steps in the fabrication of a device. The method of finishing the device will depend entirely on the application. Two possible areas of application are discussed below with reference to Figures 10-12.

Trench Gated Power Devices

These are vertical devices which are all connected in parallel to allow large current conduction. Such devices can be capable of withstanding thousands of volts and conducting hundreds of amps. Examples of such devices are power MOSFETs (Metal Oxide Semiconductor Field Effect Transistors), MESFETs (Metal Semiconductor Field Effect Transistors) and IGBTs (Insulated Gate Bipolar Transistors.

Two examples are shown in Figures 10 and 11. Figure 10 shows a power MOSFET device and Figure 11 shows a power IGBT. Both trenches are formed on a substrate with a heavily doped lower layer 14, (n+++ in the case of the MOSFET and p+++ in the case of the IGBT), with an n- drain drift region 15 and a p base region 16. The doped lateral regions 8 are n++ source regions. In the case of the power MOSFET (Figure 10) the trench is filled with an oxide 17, the electrode 18 acts as a source, electrode 19 acts as a drain and the trench electrode 5 acts as a gate. In the case of the IGBT (Figure 11), the upper electrode 20 acts an emitter and the lower electrode 21 acts as a collector. In both cases, the polysilicon layer 5 acts as a gate.

Logic Transistors and Memory Cells

Figure 12 illustrates a logic transistor or memory cell which has been formed from the trench device previously described in Figures 1 to 9. The trench is formed in a substrate comprising a p base region 22. The laterally doped regions 23,24 are n+ regions. An oxide layer 25 is formed in the upper region of the trench. A passivation layer 26 is formed above the oxide layer. Source 27 and drain 28 electrodes are also provided. Trench electrode 29 acts as a gate.

For better operation, the trench in this device may well penetrate into a highly conductive epitaxial layer.

All of the above devices can have the p regions swapped for n, and vice-versa for different operating characteristics.

Figure 13 illustrates the gradual drop off in doping concentration exhibited by a vertical implant (i.e. the first conventional method discussed earlier). Note the gradual vertical drop off in concentration, indicated at 30.

Figure 14 illustrates the more uniform doping concentration in the exposed area of the trench during the implant of the present invention. Note that the trench surface concentration, indicated at 31, is uniform, unlike in a conventionally doped region illustrated in Figure 13. The shadowing technique (i.e. the second conventional technique described earlier) may yield a similar profile, although there would be a significant amount of dopant material in areas which would be masked off (particularly by the material 5) during the implant of the present invention.

CLAIMS

1. A method of forming a doped trench as part of the fabrication of a semiconductor device, the method comprising:

(i) forming a trench in a semiconductor substrate using a mask to define the trench region;

(ii) either

a) filling the trench and removing part of the contents of the trench to leave a partially filled trench; or

b) partially filling the trench; and

(iii) doping the side walls of the trench with the mask still in place.

2. A method according to claim 1 further comprising forming a layer of dielectric on the surface of the trench between steps (i) and (ii).

3. A method according to claim 2, wherein step (iii) is carried out through the dielectric layer.

4. A method according to claim 2, further comprising removing the layer of dielectric from the exposed part of the trench after step (ii).

5. A method according to any of the preceding claims, wherein step (iii) comprises implanting dopant ions from an angled ionic source.

6. A method according to claim 5, wherein the angle of the ionic source to the surface of the substrate is large enough such that ionic reflections from the side walls of the trench causes substantially all sides of the trench to be at least partially doped in one implanting step.

7. A method according to any of claims 1 to 4, wherein step (iii) comprises diffusing dopant ions into the sidewalls of the trench from a dopant gas.

8. A method according to any of claims 1 to 4, wherein step (iii) comprises deposition of a dopant source.

9. A method according to any of claims 1 to 4, wherein step (iii) comprises filing the exposed part of the trench with spin on dopant.

10. A method of fabricating a semiconductor device comprising forming a doped trench by a method according to any of the preceding claims, and fabricating the semiconductor device including the doped trench.

11. A method according to claim 10 wherein the semiconductor device is one of a trench gated power device, logic transistor or memory cell.

12. A method according to claim 10 or 11 wherein the semiconductor device has a gate electrode formed in the trench.

13. A method according to any of the preceding claims, wherein the trench is partially filled in step (ii) before the doping step (iii) which dopes the side walls of the partially filled trench.

14. A method according to any of the preceding claims, wherein the trench is partially filled in step (ii) with trench electrode material.

15. A semiconductor device constructed by a method according to any of the preceding claims.

16. A device according to claim 15, wherein the device is one of a trench gated power device, logic transistor or memory cell.

17. A device according to claim 15 or 16, wherein the doped regions of the side walls of the trench have a doping concentration which is substantially uniform in the exposed part of the trench.

Fig.1.

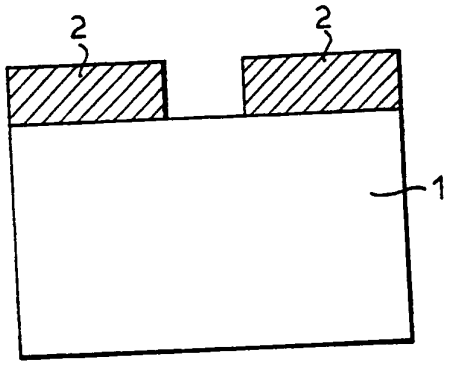


Fig.2.

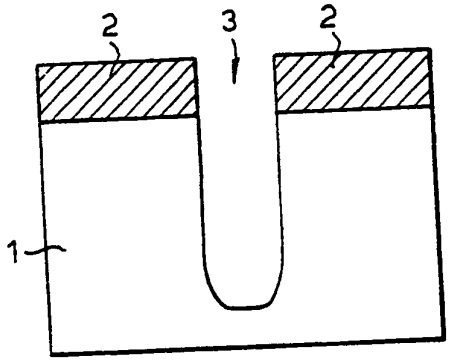


Fig.3.

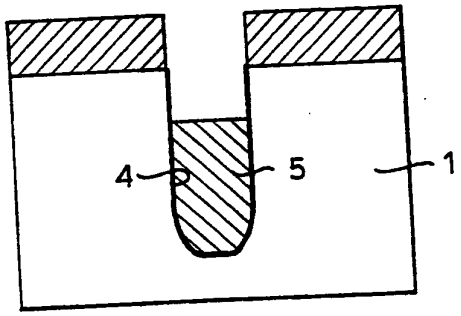


Fig.3A.

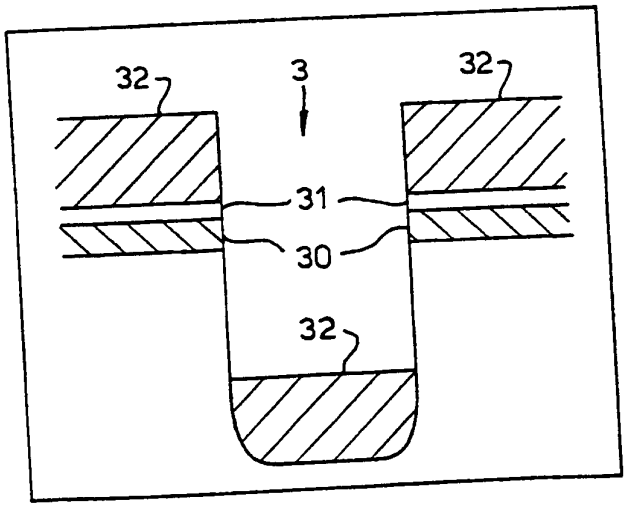


Fig.4.

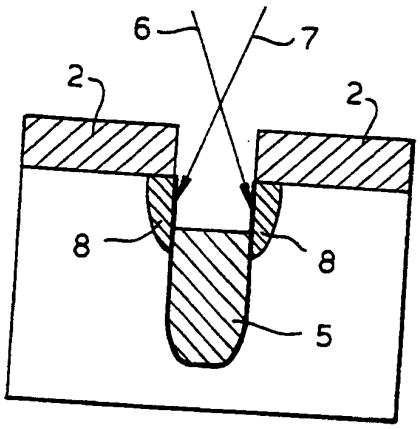


Fig.5.

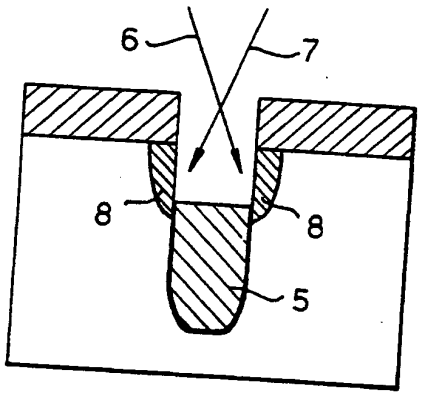


Fig.6.

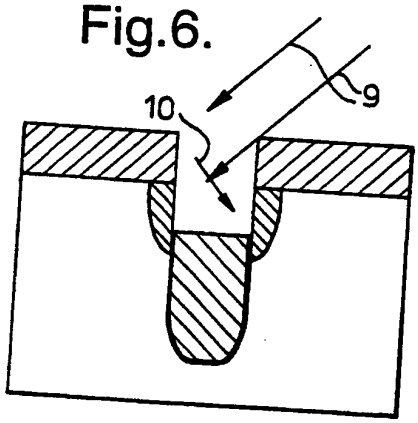


Fig.7.

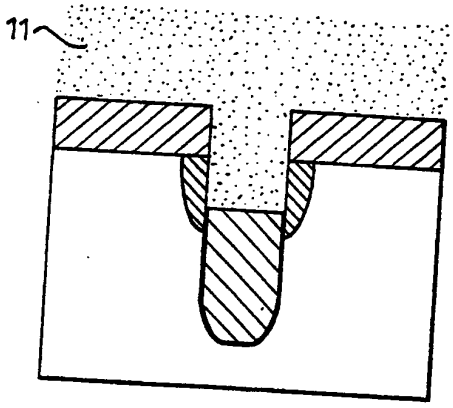


Fig.8.

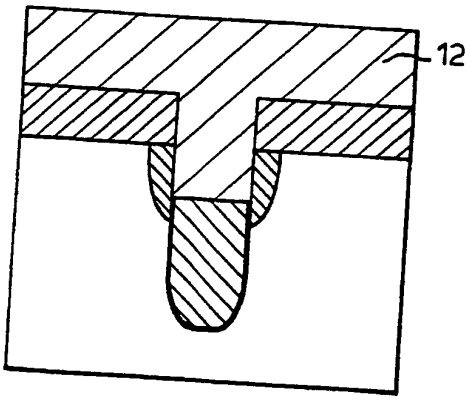


Fig.9.

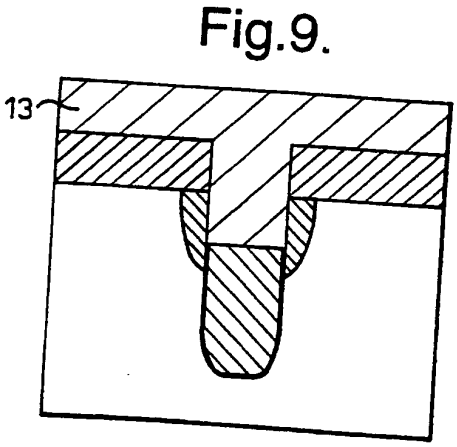


Fig.10.

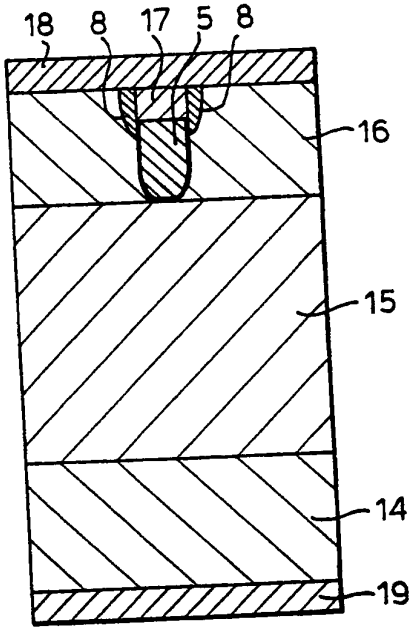


Fig.11.

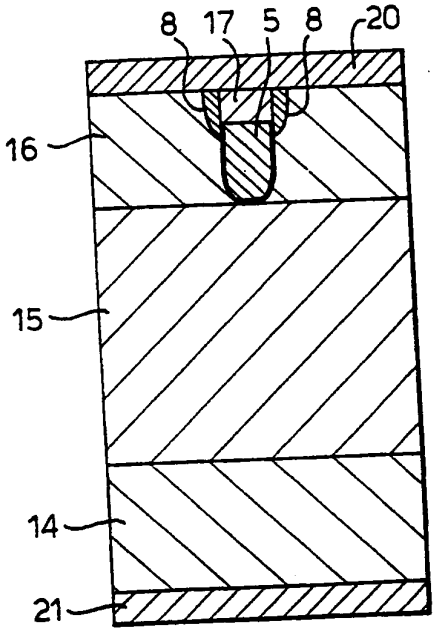


Fig.12.

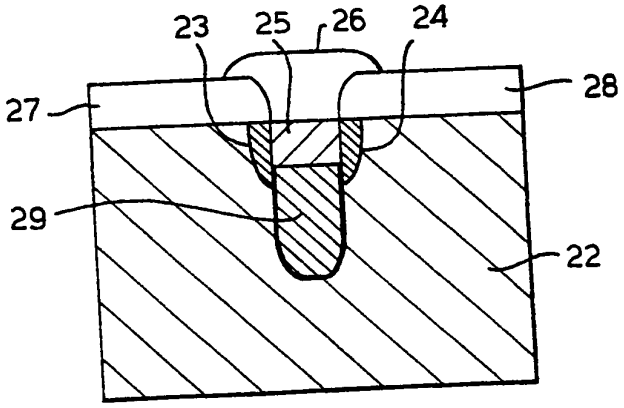
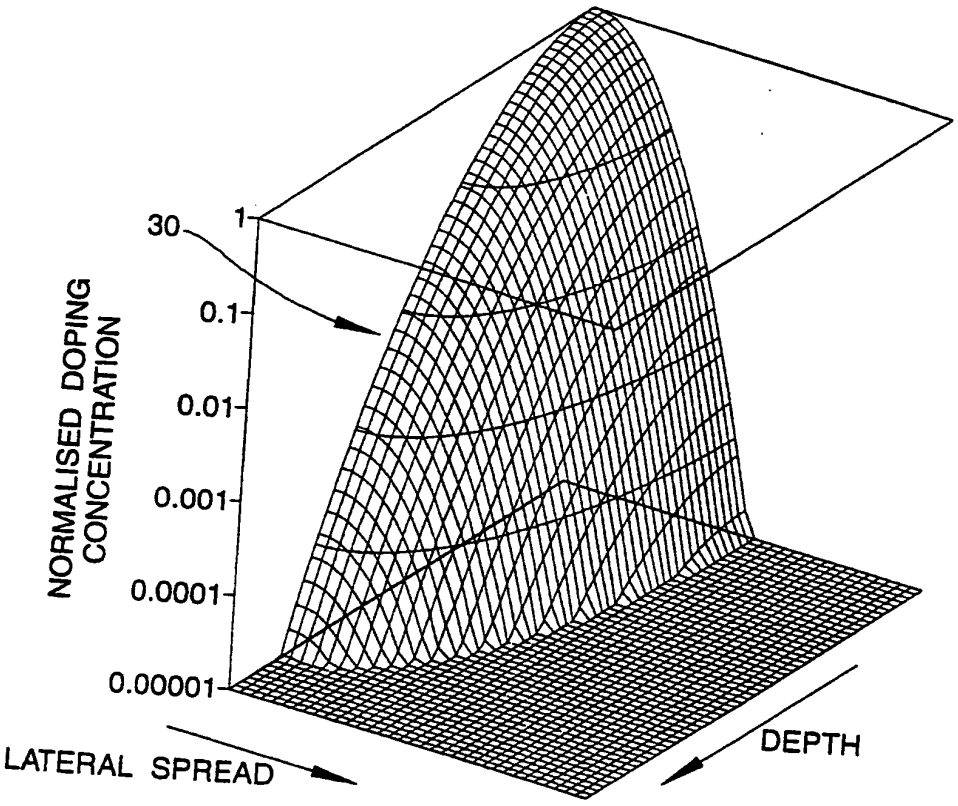


Fig.13.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NORMALISED DOPING CONCENTRATION
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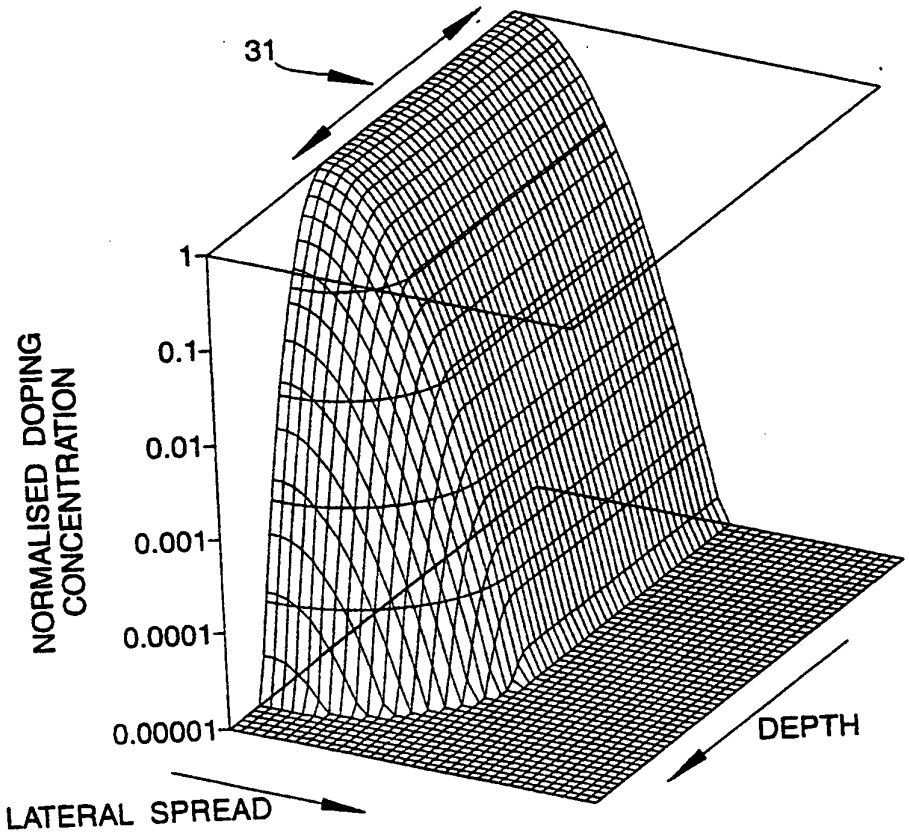
Fig.14.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NORMALISED DOPING CONCENTRATION
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INTERNATIONAL SEARCH REPORT

Inte nal Application No
PCT/GB 96/01445

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H01L21/336 H01L21/331 H01L21/265 H01L29/739 H01L29/78 H01L29/423

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H01L

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C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	PATENT ABSTRACTS OF JAPAN vol. 012, no. 168 (E-611), 20 May 1988 & JP,A,62 279666 (MATSUSHITA ELECTRIC IND CO LTD), 4 December 1987, see abstract; figures 1,2 ---	1,5,10, 11,13, 15-17
A	FR,A,2 647 596 (FUJI ELECTRIC CO LTD) 30 November 1990 see page 6, line 9 - page 10, line 9; figures 1,2 ---	1,2,4,8, 10-17
A	GB,A,2 264 388 (MITSUBISHI ELECTRIC CORP) 25 August 1993 see figures 1-15 ---	1,2,4,8, 10-17
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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
12 September 1996	25. 09. 96

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax (+31-70) 340-3016	Gêlêbart, J

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INTERNATIONAL SEARCH REPORT

Int onal Application No
PCT/GB 96/01445

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	PATENT ABSTRACTS OF JAPAN vol. 013, no. 348 (E-799), 4 August 1989 & JP,A,01 108762 (MATSUSHITA ELECTRIC IND CO LTD), 26 April 1989, see abstract; figures 1,2	1-3,5, 10-17
A	EP,A,0 221 593 (PHILIPS NV) 13 May 1987 see page 5, line 3 - page 7, line 34; figures 5-8,11	1-3,5, 10-12, 15-17
A	EP,A,0 234 244 (SIEMENS AG) 2 September 1987 see abstract; figure	1,5,6, 10,11, 15-17
A	APPLIED PHYSICS LETTERS, vol. 54, no. 16, 17 April 1989, pages 1534-1536, XP000032138 FUSE G ET AL: "INDIRECT TRENCH SIDEWALL DOPING BY IMPLANTATION OF REFLECTED IONS" see abstract; figure 1	1,5,6, 10,11, 15-17

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INTERNATIONAL SEARCH REPORT

Information on patent family members

Int ional Application No
PCT/GB 96/01445

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